### PATENT COOPERATION TREATY

## **PCT**

# TRANSLATION INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P37427-P0	FOR FURTHER ACTION	See Form PCT/IPEA/416			
International application No.	International filing date (day/month/year)	Priority date (day/month/year)			
PCT/JP2005/003136	25.02.2005	27.02.2004			
International Patent Classification (IPC) or national	onal classification and IPC				
G06F12/16 (2006.01)					
Applicant					
MATSUSHITA ELECTRIC	INDUSTRIAL CO., LTD.				
	1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.				
2. This REPORT consists of a total of	6 sheets, incl	uding this cover sheet.			
This report is also accompanied by Al					
a. (sent to the applicant and	to the International Bureau) a total of 1	sheets, as follows:			
		een amended and are the basis for this report and/or			
sheets containing red Instructions).	sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).				
	sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond				
the disclosure in the Box.	the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.				
b. (sent to the International i	Bureau only) a total of (indicate type and nu	nmber of electronic carrier(s))			
, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see					
Section 802 of the Administ	rative Instructions).				
4. This report contains indications relating	ng to the following items:				
Box No. I Basis of the	report				
Box No. II Priority					
Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability		eventive step and industrial applicability			
Box No. IV Lack of unit	y of invention				
BOX 110. 1	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement				
Box No. VI Certain doct	Box No. VI Certain documents cited				
Box No. VII Certain defe	ects in the international application				
Box No. VIII Certain obse	ervations on the international application				
Date of submission of the demand	Date of completion	of this report			
		-			
Name and mailing address of the IPEA/JP	Authorized officer				
Facsimile No.	Telephone No.				

International application No.

PCT/JP2005/003136

Box	No. I	Basis of the report		
1.		n regard to the language, this report is based on the internation cated under this item.	nal application in the language in	which it was filed, unless otherwise
		This report is based on translations from the original language which is the language of a translation furnished for the purposition international search (Rule 12.3 and 23.1(b))  publication of the international application (Rule 12.4) international preliminary examination (Rule 55.2 and/	oses of:	,
2.	rece	n regard to the <b>elements</b> of the international application, this iving Office in response to an invitation under Article 14 are report):  the international application as originally filed/furnished the description:	e referred to in this report as "o	riginally filed" and are not annexed to
				as originally filed/furnished
				_
	$\square$		received by this Authority on	
		the claims:		and simplify Glad/Granish ad
				as originally filed/furnished
		nos.* nos.* _1		
		nos.*		
	$\boxtimes$		received by this ridinority on	_
	K_N	the drawings: sheets Fig. 1–12		as originally filed/furnished
		sheets*		
		sheets*		-
	П	a sequence listing and/or any related table(s) – see Supplem		
3.	$\boxtimes$	The amendments have resulted in the cancellation of:		
٥.				
		the claims, nos. 4		
		41-1		_
				_
4.		This report has been established as if (some of) the amend they have been considered to go beyond the disclosure as fil	ments annexed to this report and	listed below had not been made, since
		the description, pages		
		the claims, nos.		
		the sequence listing (specify):		
		any table(s) related to sequence listing (specify):		
*	If ite	em 4 applies, some or all of those sheets may be marked "supe	erseded."	

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Box			dicle 35(2) with regard to novelty, inventive step or industrial applicability; oporting such statement	
1.	Statement			
	Novelty (N)	Claims	1□3, 5-13	YES
		Claims		NO
	Inventive step (IS)	Claims		YES
		Claims	1-3, 5-13	NO
	Industrial applicability (IA)	Claims	1-3, 5-13	YES
		Claims		NO NO

#### 2. Citations and explanations (Rule 70.7)

Document 1: JP 2001-5928 A (Hitachi Maxell, Ltd.), 12

January 2001, entire text; all drawings

(Family: none)

Document 2: JP 2003-15929 A (Matsushita Electric Industrial Co., Ltd.), 17 January 2003, entire text; all drawings & US 2003-189860 A1 & EP 1403771 A1 & WO 03-3219 A1 & CA 2420986 A & CN 1465012 T

The invention set forth in claims 1 to 3 and 5 to 13 does not involve an inventive step in the light of documents 1 and 2 cited in the international search report.

Document 1 sets forth an IC card which is electrically writable and is provided with a nonvolatile data storage unit which stores data in predetermined units, wherein nonvolatile memory which stores a first table for converting a logic block address specified for data access from a higher-order device into an actual block address which is an actual address in the memory space of the data storage unit which comprises a plurality of flash memories, and a second table for

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

storing flag information for managing the state of data in the actual block address, is faster than EEPROM and flash memory; and FRAM which is capable of rewriting data in byte units, or SRAM backed up by battery are used; that when transfer of predetermined block data to the data storage unit is completed, the flag information of the second memory is set to "OOH"; if a power supply interruption occurs during writing to flash memory, the status of the writing-in-progress flag is verified in the initialization after turning on the power to the IC card, and if the flag is set, the judgment is made that processing has been aborted during data writing in the previous process. In addition, document 2 sets forth a method for controlling nonvolatile memory, wherein while overwriting blocks, if a forced abort occurs due to a reset command or a power supply interruption to the storage device, a disable flag and enable flag to manage the deleting and writing of data are provided in block units which are storage capacity units which divide up nonvolatile memory into a plurality of units.

#### Claim 1

The "data storage unit", "first table" and "microcomputer" set forth in document 1 correspond to the "nonvolatile main memory", "address management information storage unit" and "control unit" of claim 1 respectively.

Moreover, it would be easy for a person skilled in the art to conceive of providing flag information for managing the status of data within the actual block address in second storage capacity units which are smaller than first storage capacity of the main storage

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

memory in the light of document 2.

#### Claims 2 and 3

Determining the nature of storage capacity units to which writing-complete flags are provided would merely be a design matter to a person skilled in the art, and employing cluster size or sector size as said unit would not be technically difficult to a person skilled in the art.

#### Claim 5

As stated above, document 1 indicates that the writing speed of control memory is faster than that of main storage memory.

#### Claims 6 and 7

When a control unit constitutes a memory map of the writing-complete flag table, constituting a pre-stored second storage capacity unit or a second storage capacity unit transferred from a host would merely be a design matter to a person skilled in the art.

#### Claims 8 and 9

It would not be particularly difficult for a person skilled in the art to have a multi-valued NAND flash memory serve as main storage memory per se. Moreover, document 1 indicates that that said memory has an address conversion table, as stated above.

#### Claims 11 to 13

It would merely be a design matter to a person skilled in the art to employ ferroelectric memory,

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Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
magnetic recording nonperiodical writing/reading memory,
ovonic unified memory or resistance RAM as control
memory.